Assignee: Intel Corporation
Docket No.: 2207/10377

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S)	:	Jeffrey F. Harness, et al.
SERIAL NO.	:	09/750,090
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FOR	:	Digital Low Pass Filter
GROUP ART UNIT	:	2124
EXAMINER	:	Chat C. Do

M/S: APPEAL BRIEF - PATENT
COMMISSIONER FOR PATENTS
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ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF

Dear Sir:

This reply brief is in response to the Examiner's Answer of January 22, 2008.

Response to Arguments Presented in the Examiner's Answer

At the outset, it is noted that the disclosure (esp. Col. 5, lines 31-45) of the cited Obinata reference (US 5,034,744) is directed to correcting for a particular glitch found in a Philips TDA 1541S1 DAC (See Col. 3, lines 14-18 and lines 46-53). Looking at Fig. 1, values O_1 to O_4 are provided to D-type flip-flops 30-33. Looking at Fig. 1, and Col. 4, lines 47-57, it is clear that a comparison is made between a sample bit (i.e., the input into one of the D-type flip-flops) and the previous sample bit (i.e., the output of the same D-type flip-flop). Looking at D flip-flop 33, the comparison is made by XOR gate 37. If both inputs to this gate are the same, then the output will be a logic "0." If both inputs to this gate are different (indicating a glitch), then the output will be a logic "1" (or "H" as stated in Obinata).

Thus, the comparison that is being made is between one bit and one bit that is adjacent to it and not "detecting a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit" as recited in the claim 1 with similar language in each of the other rejected claims. In the Examiner's Answer, at pg. 7, it states that Col. 5, lines 31-45 specifically address detecting adjacent bits on both sides of a sample bit. "The detection of difference logic level from the first side of glitch is done in col. 5 lines 31-33 for detecting difference logic level from '0' to '1' and stored to AND gate 40 as 'H.' The detection of difference logic level from the second side of glitch is done in col. 5, lines 33-36 for detecting difference logic level from '1' to '0' and stored to AND gate 41 as 'H.' These values of AND gates are later used to enable an inverting means for removing/suppressing the glitch if both of AND gates are 'H.'"

First of all, the cited section of Obinata is referring to points P_1 to P_{26} shown in Fig. 3 and referring to how the bit 4SB can change from a '0' to a '1' or a '1' to a '0.' In particular, points P_1 to P_{26} shown in Fig. 3 represent the 26 possible glitches from the DAC of the TDA1541S1 (Col. 3, lines 25-26). Accordingly, the situation where the output of AND gate 40 becomes 'H' is when the circuit is dealing with glitches represented in Fig. 3 between points P_1 to P_{13}, and the situation where the output of AND gate 41 becomes 'H' is when the circuit is dealing with glitches represented in Fig. 3 between points P_{14} to P_{26}. In other words, the AND gates 40 and 41 are dealing with different glitches and not the first side of a glitch and a second side of a glitch as stated in the Answer. As stated throughout Appellants' Brief and responses to previous Office Actions, the only glitch that Obinata is concerned with is the glitch that can be detected by the D flip-flops 30-33 and XOR gates 34-37 of Fig. 1 – a difference between one bit and one of its adjacent bits.

Second, AND gates are not storage devices, they are logic gates that change as quickly as possible after inputs to these gates change. According to the Answer, "[t]hese values of AND gates are later used to enable an inverting means for removing/suppressing the glitch <u>if both of AND gates are 'H.'</u>" (emphasis supplied). A careful review of Fig. 1 reveals that this interpretation of Obinata is simply incorrect. Note that AND gates 40 and 41 are each three-input AND gates. The first input of both AND gates is the output of XOR gate 37. The third input of both AND gates is the output of NAND gate 39. The second input of AND gate 40 is the output of XOR 42 while the second input of AND gate 41 is the <u>inverted</u> (by inverter 43) output of XOR 42. Though the outputs of AND gates 40 and 41 may be '0' or low at the same time, they can never be '1' or 'H' at the same time, because the second input of these gate will always be '0' for one of these AND gates 40 and 41.

In view of the above, Appellants respectfully submit that the rejection of claim 1, 7-10 and 19 under 35 U.S.C. §§ 102(b) and 103(a) is in error and should be reversed.

CONCLUSION

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1, 7-10 and 19 under 35 U.S.C. §§ 102(b) and 103(a) and direct the Examiner to pass the case to issue.

The Commissioner is hereby authorized to charge any fees which may be necessary for consideration of this Reply Brief to Kenyon & Kenyon Deposit Account No. 11-0600. A copy of this sheet is enclosed for that purpose.

Respectfully submitted,

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